Exhibit

# IMPACT OF MNOS/AWSI TECHNOLOGY ON REPROGRAMMABLE ARRAYS

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## ABSTRACT

Adaptive Wafer Scale Integration (AWSI) is an interconnected net of arrays. The interconnection is a reprogrammable bus. All components, including active and spare arrays, bus lines, and bus interconnects, are fabricated on the same semiconductor wafer substrate. Nonvolatile interconnect circuits serve as controllers for address, power, and data bus lines. Under the control of error management hardware, the interconnect circuits enable malfunctioning arrays to be replaced automatically by integral spare arrays. Since the interconnects are insitu alterable, this sparing process can be carried out repetitively when required.

Initial empirical validation of the ASWI was accomplished with a reconfiguration memory wafer based on N channel Metal Nitride Oxide Semiconductor (MNOS) process technology and AWSI interconnect mechanization. More recently, an MNOS/CMOS process was developed. Examples of MNOS/AWSI applications are highlighted. In addition, the relationship of MNOS/AWSI to the VHSIC Program objectives are discussed.

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## 1. INTRODUCTION - THE MNOS/AWSI TECHNOLOGY

The MNOS/AWSI technology[1] is a system approach to further military electronic technology toward ever improving cost effectiveness of military systems as well as enhancement of operation capabilities and performance. Through the years, for the same electronic functions, the cost of the system has dropped by orders of magnitude even as the performance of the system improves with continuing reductions in weight, volume, and power. The MNOS/AWSI employs electrically alterable, nonvolatile interconnect controller circuits processed into a semiconductor wafer to connect "arrays" of interconnected, operable circuits (also processed into the wafer) to a bus structure deposited on the wafer between the arrays. With this approach, AWSI can have important advantages relative to other high density electronic circuit approaches. Such advantages are the direct consequences of wafer scale integration based on (1) the electronic reconfigurability of interconnect circuits, and (2) the compatibility of the MNOS with the N channel MNOS and CMOS LSI and VLSI semiconductor processes. MNOS/AWSI advantages include process yield enhancement, system reliability improvement, and performance features such as self-healing and fault tolerance; plus reduction in size, weight, and cost.

The AWSI concept is first contrasted with conventional integrated circuit (IC) technology: In both technologies the "chip" or "dice" (called arrays in AWSI) are probed immediately after the completion of wafer processing to test for operability. In conventional IC technology, those dice which do not pass the probe tests are marked and discarded when the wafer is diced into individual chips. The probe-test accepted dice are then typically packaged and retested prior to shipment to a separate organization or industrial entity. The packaged dice are subsequently subjected to incoming inspection and acceptance. Those that passed are assembled and interconnected on a circuit board to constitute the electronic unit or subsystem.

In AWSI, the arrays are all connected via system bus. The address of those arrays that pass the probe test are stored in nonvolatile memory. Operable arrays which are initially used in system mechanization are

accessible either via indirect addressing or via associative decoder addressing. The remainder of the operable arrays are reserved as spares to be connected into the bus structure as replacements for operating arrays which subsequently may be shown by built-in-tests to have become defective. Alternatively, the spares can be later used for system reconfiguration dependent on application requirements.

The AWSI wafer, either as a whole, or in segments of interconnected multiple array units, are packaged in large "chip" carrier packages. These AWSI package units are the equivalent of circuit boards in conventional integrated circuit electronic packaging techniques.

The use of a repeatedly alterable, electrical interconnect, processed into the wafer provides the principal advantages of AWSI compared to other whole-wafer technologies.[2-7] With AWSI interconnect*:

a. Any array may be connected to, or disconnected from, the bus structure at any time; connections include both signals and power.
b. Neither nonoperable nor nonoperating arrays draw power.
c. Neither special contact masks, metallization masks nor fusible links are required to connect arrays to bus lines. Conditional interconnect is accomplished electronically instead of via nonalterable mechanical means.
d. Spare operable arrays are stored on the wafer and connected to the bus structure whenever built-in-tests reveal that one of the active arrays has failed and must be replaced.
e. Reconfiguration may be achieved within limits established via the system architecture by reconnecting arrays to the interconnect bus.

## 2. BASIS FOR AWSI

The technological basis for the AWSI interconnect is the nonvolatile semiconductor memory transistor, the MNOS transistor.[8-11]

The MNOS transistor is unique among solid-state electronic devices

*Y. Hsia, "Associative Interconnection Circuit", US Patent No. 4,188,670

in that it permits stored data alterability simultaneously with stored data nonvolatility. It also provides a small area structure and fabrication compatibility with high density, integrated circuit technologies.

The MNOS transistor is a close relative of the conventional Metal-Oxide-Semiconductor (MOS) transistor in that the usual layer of gate oxide is replaced by a 400Å layer of silicon nitride over a less than 20Å thick layer of silicon dioxide, Figure 1. The application of a moderately-high voltage (approximately 20-25 volts) to the gate electrode of this transistor causes the thin silicon dioxide layer to become conductive (or to permit charge carriers to tunnel through it). Charge carriers may then pass between the silicon and charge-carrier traps located in the silicon nitride near the silicon nitride, silicon dioxide interface. The presence of trapped charge carriers at this interface modifies the gate voltage which controls passage of charge carriers from source to drain in the conventional operation of the transistor. The MNOS transistor is then said to have an off and an on state which depends on the concentration and the polarity of the trapped charge carriers, Figure 2.

The MNOS transistors, utilized in a circuit, effectively became the means with which electrically alterable interconnection can be implemented in place of mechanically hardwired interconnections. The alterable interconnect can be so utilized because the interconnection has a nonvolatile memory for status control so that the state of an interconnected machine is static as if hardwired. Yet it is alterable (that is adaptive), via control signals by circuit means.

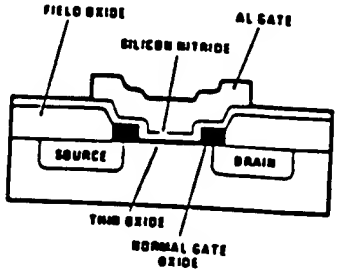


Figure 1. Schematic showing representative section through MNOS memory transistor.

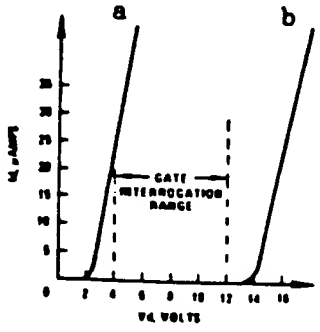


Figure 2. Transfer characteristics of an MNOS transistor.
(a) High conductance state
(b) Low conductance state

The adaptive feature of the interconnect makes it possible to implement sparing to produce high reliability memory systems. A minimum number of spare memory circuits is set aside on the wafer. Upon detection of a failure, the defective component is disconnected and the spare is connected to the system bus. Utilizing sparing redundancy, high system reliability is accomplished with minimum hardware cost and little increase in parts count. An illustrative example is given in Figure 3. Assume 16 memory circuits interconnected to form a high reliability memory subsystem, assigning the same failure rates to equivalent-function units, it can be seen that using two spares for a 16-unit serial memory system, an order of magnitude improvement in calculated failure rate is achieved over that utilizing the dual-redundant approach. The improvement is impressive since the sparing redundancy is realized with reduced hardware and minimum operating power.

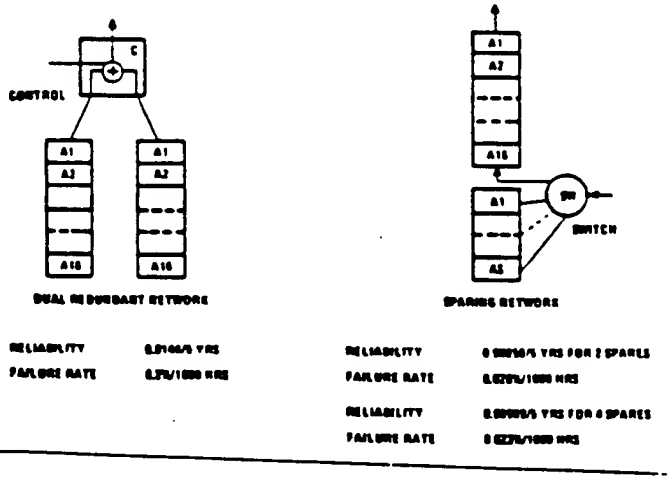


Figure 3. Example of gain in reliability with the use of sparing redundancy..

As an introduction to the AWSI concepts to concrete physical terms, we can use the example of an early feasibility demonstration vehicle, the reconfigurable memory wafer circuit, RMWC-1, Figure 4. The interconnect is composed of an electrically alterable, nonvolatile, MNOS memory cell and a standard logic date transistor circuit or bus controller. The bus controller is enabled by the enabling signal which is conditional on the

stored interconnect status of the memory cell. The bus controller connects or gates the power, clock and data signals from the interconnecting bus to the engaged circuit, in this case, a shift register. The relationship of the MNOS memory cell, the bus controller, and the shift register in the AWSI implementation is shown in Figure 5.

A study reveals that mass memory presents a most exciting application for the MNOS/AWSI technology.[12] Storage nonvolatility is achieved with semiconductor memory and concurrently, the many system advantages of AWSI is fully utilized for the application.

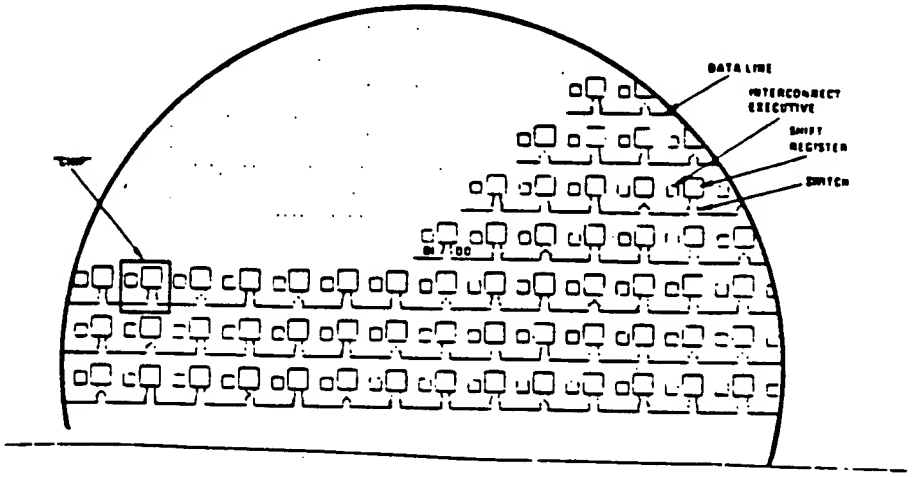


Figure 4. Data path organization of RMWC-1.

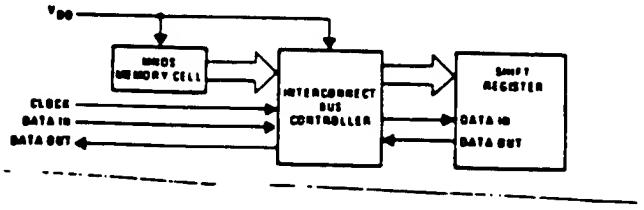


Figure 5. Use of AWSI to interconnect a shift register string.

## 3. THE RECONFIGURABLE MEMORY WAFER

As a first step toward the implementation of a memory wafer for mass memory application, a reconfigurable memory wafer (MAW-1) was developed and studied. The MAW-1 is composed of interconnected memory arrays for the purpose of evaluating the circuits necessary to accomplish power switching, address storage and decode address control for interconnect reconfiguration. Figure 6 is an overview of the MAW-1 which shows the physical arrangement of the device. Figure 7 is a photomicrograph of the MAW-1 circuit array illustrating also the wafer-level interconnect, or the macrobus.

A 4096-bit nonvolatile sequential access memory (SAM) was the basic memory storage array.[13] Several features of the SAM array uniquely establish its application in an AWSI memory:

a. Memory storage is nonvolatile, based on N channel MNOS storage.
b. Data input is high impedance and buffered with an input latch. Data output is tri-state, and buffered for bus driving.
c. To reduce interconnect bus lines, access within the SAM storage array is sequenced internally, timing input is restricted to a single clock line, and operation instructions are decoded internally.
d. For multiplexed operation in a bus interconnected system, a chip select control, and a flag bit are provided..

The mechanization of on-the-wafer interconnect is accomplished with the development of an associative interconnect. The associative interconnect consists of six major components:

a. The macrobus, which is the system bus.
b. Power switches.
c. Power connect/disconnect logic.
d. Nonvolatile address memory.
e. Address memory control.
f. Address comparators.

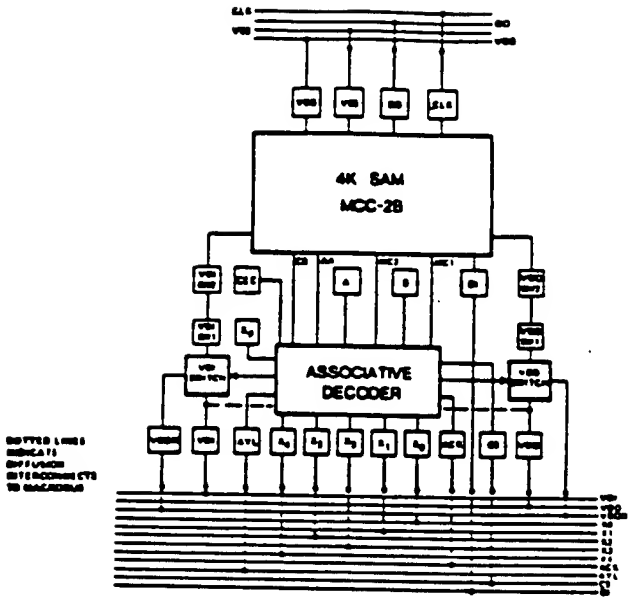


Figure 6. MAW-1 overview: associative decoder, SAM with internal parts, and macrobus.

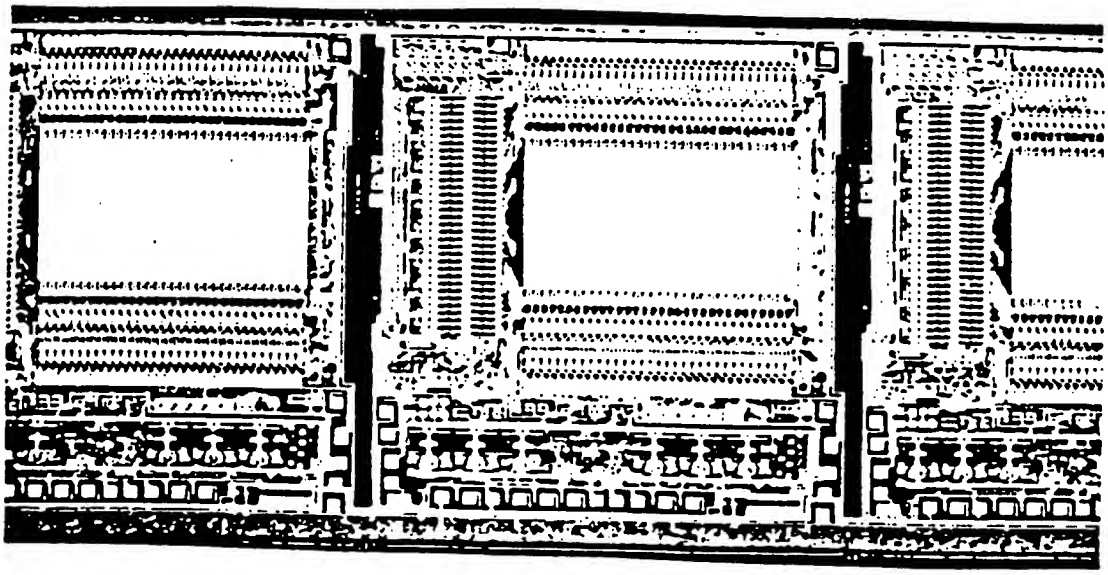

Figure 7. Photomicrograph of MAW-1; the wafer-level interconnected 4096-bit sequential access memory.

The associative interconnect was tested for and successfully demonstrated (1) address memory storage and pattern insensitivity, (2) power-on control to the SAM by associative decoder address match and mismatch, (3) power turnoff of the SAM by address match, (4) permanent programmable match disable to eliminate bad decoder circuits and/or SAM's, and (5) power response time of 5 microseconds.

With the associative interconnect tested for operation, the MAW-1 was tested and demonstrated (1) selective power switching via the macrobus, (2) selective control of SAM circuit operation (read, write, and erase) from the macrobus, and (3) lockout of defective SAM's. The successful completion of the MAW-1 tests leads to the next step of effort, the development of the AWSI MNOS solid-state memory which is in progress at MDC.

## 4. AN MNOS/AWSI SOLID STATE MASS MEMORY

AWSI on-the-wafer interconnect is mechanized such that small single-chip sequential access memory arrays (with memory storage capacity of 8K bits per memory array) are interconnected to result in a large capacity store (greater than $10^5$ bits) in a single slice of silicon wafer. The use of nonvolatile memories as the storage array in a mass memory system results in very low system power as compared with other semiconductor memories. Power need be applied only to those storage arrays accessed with no standby power necessary to maintain data in unaccessed storage arrays. Additionally, with the use of AWSI sparing redundancy, the mass memory achieves high system reliability at low cost.

The memory system can be divided into wafer memory modules and memory control circuitry. The wafer memory modules consist of memory wafer slices which, in turn, consist of the array controllers (AC), the memory arrays (MA), and the buses which connect them. Figure 8 shows the memory wafer slice.